# UNITED STATES PATENT APPLICATION

# SEMICONDUCTING DEVICE WITH FOLDED INTERPOSER

## INVENTOR

Iwen Chao

Steve R. Eskildsen

Schwegman, Lundberg, Woessner, & Kluth, P.A.
1600 TCF Tower
121 South Eighth Street
Minneapolis, Minnesota 55402
ATTORNEY DOCKET 884.C26US1
Client Ref. No. P18818

### SEMICONDUCTING DEVICE WITH FOLDED INTERPOSER

#### **Technical Field**

Some embodiments of the present invention relate to a semiconducting device, and in particular, to a semiconducting device that includes multiple dice attached to a folded interposer, and to manufacturing methods related thereto.

## **Background**

High performance semiconducting devices are continually being redesigned in order to increase processing speed and/or power. Each increase in processing speed and power generally carries a cost of increased size such that additional innovations must be made in order to minimize the size of the semiconducting devices. Manufacturers of semiconducting devices constantly try to improve product performance and reduce product size while minimizing production costs. A typical semiconducting device includes a die that is mounted on a substrate which functionally connects the die through a hierarchy of electrically conductive paths to the other elements that make up an electronic system.

Several methods have been employed to minimize the size of semiconducting devices. One method includes placing one or more dice onto an interposer and then folding the interposer to place one die on top of another.

One drawback of a semiconducting device that includes a folded interposer is that it is difficult to deliver power and/or signals to each of the dice because all of the conductive paths must be crowded through the fold in the interposer.

Therefore, as the size of a semiconducting device decreases, it becomes more difficult to deliver signals and power to the dice through the fold in the interposer.

One way to address crowding within the fold in the interposer is to make the conductive paths smaller and place them closer together. However, when the conductive paths are small and crowded together, there is increased resistance, inductance and crosstalk within the conductive paths. This increased resistance,

5

10

15

20

inductance and crosstalk causes unwanted signal degradation and power loss that inhibit the performance of the semiconducting device.

## **Brief Description of the Drawings**

- FIG. 1 is a schematic section view of a semiconducting device that includes multiple dice on a folded interposer.
  - FIG. 2 is a perspective view illustrating the semiconducting device of FIG. 1.
- FIG. 3 is a perspective view illustrating another semiconducting device that includes multiple dice on a folded interposer.
  - FIG. 4 is a schematic section view of another semiconducting device that includes multiple dice on a folded interposer.
  - FIG. 5 illustrates a method of fabricating a semiconducting device that includes multiple dice on a folded interposer.
- FIG. 6 is a schematic section view illustrating portions of the semiconducting device shown in FIG. 1 prior to folding.
  - FIG. 7 is a schematic section view illustrating the portions of the semiconducting device shown in FIG. 6 after folding.
- FIG. 8 is a block diagram of an electronic system that incorporates at least one semiconducting device of the type shown in FIGS. 1-7.

### **Detailed Description**

In the following detailed description, reference is made to the accompanying drawings. In the drawings, like numerals describe substantially similar components throughout the several views. Other embodiments may be utilized, and structural, logical, and electrical changes may be made.

FIGS. 1 and 2 illustrate a semiconducting device 10 that includes a first die 12 and a second die 14. The semiconducting device 10 further includes an interposer 16 that has a fold 18 which divides the interposer 16 into a first section 20 and a second section 22. First die 12 is attached to a first surface 24 of interposer 16

25

at first section 20 and second section 22. Second die 14 is attached to a second surface 25 of interposer 16. Second die 14 is stacked onto first die 12 and is electrically coupled to first die 12 by at least one contact 26 and conductive paths (not shown) that are part of interposer 16. Contacts 26 are attached to the first surface 24 of interposer 16 at first section 20 and second section 22.

It should be noted that the arrangement of the first and second dice 12, 14 relative to one another will depend on a variety of circuit design factors. The first and second dice 12, 14 may be encapsulated by any known procedure, such as molding and sealing. The thickness of first and second dice 12, 14 may be about 0.2 millimeter (mm) and the thickness of interposer 16 may be about 0.1 mm.

Other fabrication processes such as wire bonding, lead bonding and bump bonding to conductors (not shown) in the interposer 16 may be done to first and second dice 12, 14 prior to encapsulation. In addition, first and second dice 12, 14 may be subjected to additional processes such as ball attaching and/or marking after encapsulation. It should be noted that semiconducting device 10 may include additional dice (not shown) formed on first and second surfaces 24, 25 of interposer 16.

The first and second dice 12, 14 may be secured to the first and second surfaces 24, 25 of interposer 16 using an adhesive, a conductive epoxy or some form of solder attachment (among other methods). FIG. 1 illustrates that first die 12 is secured to first surface 24 of interposer 16 at first section 20 and second section 22.

As shown in FIGS. 2-4, semiconducting device 10 may include a plurality of contacts 26 that are each attached to the first surface 24 of interposer 16 at first section 20 and second section 22. In some embodiments, fold 18 is on one side of first die 12 and at least one of the contacts 26 is on an opposing side of first die 12 (FIGS.1 and 2). In other embodiments, at least one of the contacts 26 is on some, or all, sides of first die 12. In FIGS. 3 and 4, contacts 26 are visible on only two sides of first die 12 because of the orientation of the FIGS.

The plurality of contacts 26 provides additional conductive paths for delivering signals and power between and/or to first and second dice 12, 14. The

5

10

15

20

25

plurality of contacts 26 may also decrease the overall distance of many of the conductive paths within semiconducting device 10 depending on the design of the semiconducting device 10.

In the example embodiments illustrated in the FIGS. 1-4, each of the contacts 26 is a solder column. It should be noted that any type of contact 26 may be used as long as contact 26 extends from first surface 24 of interposer 16 between first section 20 and second section 22. A number of materials may be used for interposer 16 and contacts 26. The choice of materials will depend on the relevant circuit design considerations and the costs that are associated with fabricating semiconducting device 10 (among other factors).

Referring now also to FIG. 5, an example method 50 of the present invention includes 52 securing a first die 12 to a first section 20 of an interposer 16 that has a first conductor 27A and a second conductor 27B on a first surface 24 of interposer 16 (see FIG. 6). The first die 12 may be secured to the first surface 24 of interposer 16 using solder or adhesives (among other methods).

The method 50 further includes 54 folding interposer 16 to secure first die 12 to a second section 22 of interposer 16 and to connect the first conductor 27A to the second conductor 27B to form a contact 26 (see FIG. 7). The method 50 further includes 56 securing a second die 14 to a second surface 25 of interposer 16 (e.g., by soldering) such that first and second dice 12, 14 are stacked one on top of another and electrically coupled together by interposer 16 and contact 26 (see FIG. 1).

As shown in FIGS. 1, 4, 6 and 7, folding interposer 16 to secure first die 12 to a second section 22 of interposer 16 may include placing an adhesive 30 on first die 12 and connecting the first surface 24 of interposer 16 to adhesive 30. Fold 18 may be on one side of first die 12 with first conductor 27A and second conductor 27B joined together to form contact 26 on an opposing side of first die 12 (see, e.g., FIGS. 1, 2 and 6).

In some example embodiments of the method 50, interposer 16 may include a plurality of conductors on the first surface 24 of interposer 16 such that 52 folding

5

10

15

20

25

interposer 16 includes connecting each of the plurality of conductors on a first section 20 of interposer 16 to conductors on a second section 22 of interposer 16 to form a plurality of contacts 26. Each of the contacts 26 extends from the first surface 24 of interposer 16 between first and second sections 20, 22 of interposer 16 (see, e.g., FIGS. 2-4).

Fold 18 may be on one side of first die 12 such that forming a plurality of contacts 26 includes (i) forming at least one contact 26 on an opposing side of first die 12 (FIG. 2); (ii) forming at least one contact 26 on each side of the first die 12 except for the side of first die 12 that is adjacent to the fold 18 (two sides visible in FIG. 3); and/or (iii) forming at least one contact 26 on each side of first die 12 (two sides visible in FIG.4).

Forming a plurality of contacts 26 that extend from the first surface 24 of interposer 16 between the first and second sections 20, 22 of interposer 16 increases the number of possible connections between first and second dice 12, 14 as compared to just interposer 16 alone. Method 50 may also reduce the length of the conductive paths between first and second dice 12, 14 since contacts 26 can be positioned on all sides of first die 12 instead of just through the fold 18 in interposer 16. Increasing the number of available connections, and reducing the length of the connections, may reduce resistance, inductance and crosstalk to improve signal integrity relative to first and second dice 12, 14 and power delivery to second die 14 within semiconducting device 10.

FIG. 8 is a block diagram of an electronic system 70, such as a computer system, that includes a motherboard 71 which is electrically coupled to various components in electronic system 70 via a system bus 72. System bus 72 may be a single bus or any combination of busses.

Any of the semiconducting devices 10 described herein may be mounted onto motherboard 71. Semiconducting device 10 may include a microprocessor, a microcontroller, memory, a graphics processor or a digital signal processor, and/or a custom circuit or an application-specific integrated circuit, such as a

5

10

15

20

communications circuit for use in wireless devices such as cellular telephones, pagers, portable computers, two-way radios, and similar electronic systems.

The electronic system 70 may also include an external memory 80 that in turn includes one or more memory elements suitable to the particular application, such as a main memory 82 in the form of random access memory (RAM), one or more hard drives 84, and/or one or more drives that handle removable media 86, such as floppy diskettes, compact disks (CDs) and digital video disks (DVDs).

The electronic system 70 may also include a display device 88, a speaker 89, and a controller 90, such as a keyboard, mouse, trackball, game controller, microphone, voice-recognition device, or any other device that inputs information into the electronic system 70.

In some embodiments, electronic system 70 may further include a voltage source 77 that is electrically coupled to semiconducting device 10. Voltage source 77 may be used to supply power to a die (e.g., a processor) that is within semiconducting device 10.

Semiconducting device 10 can be implemented in a number of different embodiments, including an electronic system and a computer system. The elements, materials, geometries, dimensions, and sequence of operations can all be varied to suit particular packaging requirements. Parts of some embodiments may be included in, or substituted for, those of other embodiments.

FIGS. 1-8 are merely representational and are not drawn to scale. Certain proportions thereof may be exaggerated while others may be minimized. Many other embodiments will be apparent to those of skill in the art.

The semiconducting device and method described above provide a solution for stacking dice in semiconducting packages. The semiconducting device also provides circuit designers with the availability to connect stacked dice on a folded interposer through conductive paths other than those within the interposer.

5

10

15

20